RICOH

R3121N Series

36 V Input Voltage Detector with Release Delay Function

No. EA-532-190610

OVERVIEW

R3121N is the 36 V Maximum Input Voltage Detector (Maximum Rating : 50 V). Selectable options of VDD Pin Detection Type (R3121NxxxA), SENSE Pin Detection Type (R3121NxxxE) and VDD Pin Detection without Hysteresis Type (R3121NxxxG), depending on the system configurations.

KEY BENEFITS

- Highly accurate voltage detection with detector threshold accuracy ±1.5% (Ta = 25°C)
- Selectable options of VDD Pin Detection, SENSE Pin Detection and VDD Pin Detection without Hysteresis
- Adjustment of the release delay time (Power-on Reset Time) by connecting external capacitors
- Reduction of mounting area by using compact package of SOT-23-6

KEY SPECIFICATIONS

- Operating Voltage Range (Maximum Rating) :
  R3121NxxxA/G: 1.4 V to 36.0 V (50.0 V)
  R3121NxxxE : 2.4 V to 6.0 V (7.0 V)
- Operating Temperature Range: −40°C to 85°C
- Supply Current: R3121NxxxA/G: Typ. 3.8 µA
  R3121NxxxE: Typ. 3.5 µA
- Detector Threshold Range:
  3.0 V to12.0 V (in 0.1 V step)
- Detector Threshold Accuracy: ± 1.5% (Ta = 25°C)
  2.0% (−40°C ≤ Ta ≤ 85°C)
- Release Delay Accuracy:
  −35% to 40% (−40°C ≤ Ta ≤ 85°C)

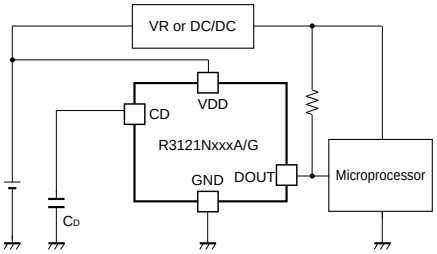
SELECTION GUIDE

Product Name	Package	Quantity per Reel
R3121Nxxx*-TR-FE	SOT-23-6	3,000 pcs

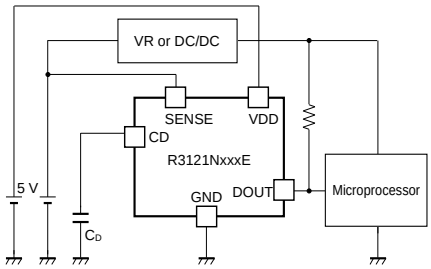
xxx: Specify the detector threshold ($-V_{DET}$) in the range of 3.0 V (030) to 12.0 V (120) in 0.1 V step

* : Select the voltage detection type
A: VDD Pin Detection Type
E: SENSE Pin Detection Type
G: VDD Pin Detection without Hysteresis Type

TYPICAL APPLICATIONS



VDD Pin Detection Type



SENSE Pin Detection Type

PACKAGES

SOT-23-6
2.9 x 2.8 x 1.1 (mm)

APPLICATIONS

- Power supply voltage monitoring for Laptop PCs, Digital TVs, Cordless phones and Private LAN systems
- Power supply voltage monitoring for devises with multi-cell battery

SELECTION GUIDE

The detector threshold and the voltage detection type are user selectable options.

Selection Guide

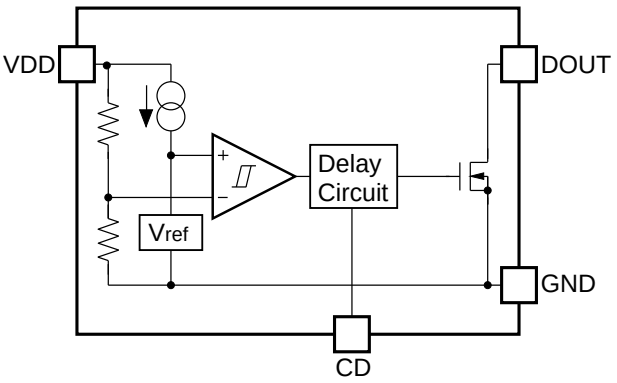
Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3121Nxxx∗-TR-FE	SOT-23-6	3,000 pcs	Yes	Yes

xxx : Specify the detector threshold ($-V_{DET}$) in the range of 3.0 V (030) to 12.0 V (120) in 0.1 V step.

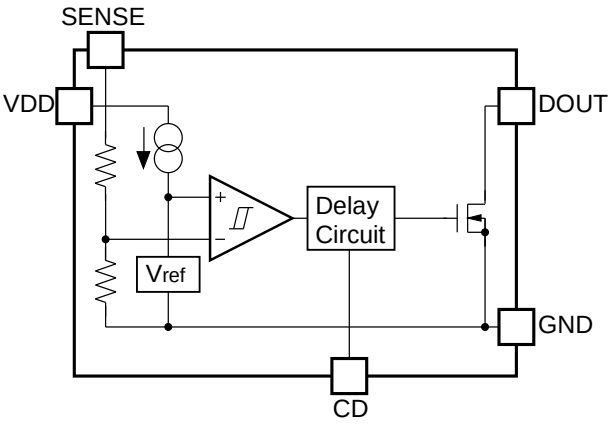
∗ : Select the voltage detection type from the following;
A: VDD Pin Detection Type
E: SENSE Pin Detection Type
G: VDD Pin Detection without Hysteresis Type

BLOCK DIAGRAMS

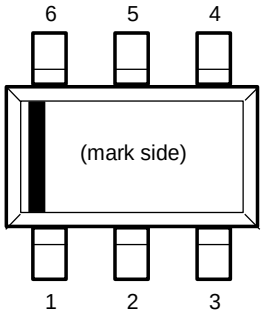
R3121NxxxA/R3121NxxxG



R3121NxxxE



PIN DESCRIPTION



R3121N（SOT-23-6) Pin Configuration

R3121N Pin Description

Pin No.	Symbol	Description
1	CD	Release Delay Time Set Pin
2	NC	No Connection
3	NC	No Connection (R3121NxxxA/R3121NxxxG)
	SENSE	VD Voltage SENSE Pin (R3121NxxxE)
4	VDD	Input Supply Voltage Pin
5	GND	Ground Pin
6	DOUT	VD Output Pin, Nch Open Drain

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Item		Rating	Unit
V_{DD}	Supply Voltage (R3121NxxxA/ R3121NxxxG)		−0.3 to 50.0	V
	Supply Voltage (R3121NxxxE)		−0.3 to 7.0	
V_{DOUT}	DOUT Pin Output Voltage		−0.3 to 7.0	V
V_{CD}	CD Pin Output Voltage		−0.3 to 7.0	V
V_{SENSE}	SENSE Pin Input Voltage (R3121NxxxE)		−0.3 to 50.0	V
I_{DOUT}	DOUT Pin Output Current		20	mA
P_D	Power Dissipation (1)	SOT-23-6, JEDEC STD. 51	660	mW
Tj	Junction Temperature		−40 to 125	°C
Tstg	Storage Temperature		−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{DD}	Operating Voltage (R3121NxxxA/ R3121NxxxG) (2)	1.4 to 36.0	V
	Operating Voltage (R3121NxxxE)(2)	2.4 to 6.0	
V_{SENSE}	SENSE Pin Input Voltage (R3121NxxxE)	0 to 36.0	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to *POWER DISSIPATION* for detailed information.
(2) Minimum value in V_{DD} indicates the minimum operating voltage to define V_{DOUT}.

ELECTRICAL CHARACTERISTICS

C_D = 1000 pF, pulled-up to 5 V with 100 kΩ, unless otherwise specified.

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

R3121NxxxA/R3121NxxxG (VDD Pin Detection Type) (Ta =25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Supply Current	V_{DD} = −V_{DET} −0.1 V		3.8	6.1	µA
		V_{DD} = +V_{DET} +1.0 V		3.8	6.4	
−V_{DET}	Detector Voltage	Ta = 25°C	x 0.985		x 1.015	V
		−40°C ≤ Ta ≤ 85°C	x 0.980		x 1.020	
V_{HYS}	Detector Threshold Hysteresis	R3121NxxxA	4.5	5	5.5	%
		R3121NxxxG	0		10	mV
t_{PHL}	Detection Delay Time(1)		40	80	140	µs
t_{DELAY}	Release Delay Time(2)		6.5	10	14	ms
I_{DOUT}	Output Current (Nch Driver)	V_{DD} = 4.5V, V_{DS} = 0.05 V	0.5		2.0	mA
R_{CDDIS}	CD Pin Discharge NMOS On-Resistance	V_{DD} = 13.0V, V_{CD} = 0.5 V	0.50		2.60	kΩ

R3121NxxxE (SENSE Pin Detection Type) (Ta =25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Supply Current(3)	V_{DD} = 5.0 V, V_{SENSE} = −V_{DET} −0.1 V		3.5	5.5	µA
		V_{DD} = 5.0 V, V_{SENSE} = +V_{DET} +1.0 V		3.5	5.6	
R_{SENSE}	SENSE Resistance		4.5		51.5	MΩ
-V_{DET}	Detector Threshold	Ta = 25°C	x 0.985		x 1.015	V
		−40°C ≤ Ta ≤ 85°C	x 0.980		x 1.020	
V_{HYS}	Detector threshold Hysteresis		4.5	5	5.5	%
t_{PHL}	Detector Delay Time(4)	V_{DD} = 4.5 V	40	80	140	µs
t_{DELAY}	Release Delay Time(5)	V_{DD} = 4.5 V	6.5	10	14.0	ms
I_{DOUT}	Output Current (Nch Driver)	V_{DD} = 5.0 V, V_{DS} = 0.05 V V_{SENSE} = −V_{DET} −0.1 V	0.5		2.0	mA
R_{CDDIS}	CD Pin Discharge NMOS On-Resistance	V_{DD} = 4.5 V, V_{SENSE}= 13.0 V, V_{CD} = 0.5V	0.50		2.60	kΩ

(1) A time that V_{DOUT} requires to reach 2.5 V when V_{DD} changes from "−V_{DET} + 1.0 V" to "−V_{DET} − 0.5 V"
(2) A time that V_{DOUT} requires to reach 2.5 V when V_{DD} changes from "−V_{DET} − 0.5 V" to "−V_{DET} + 1.0 V"
(3) Not including the current for SENSE resistance
(4) A time that V_{DOUT} requires to reach 2.5 V when V_{SENSE} changes from "−V_{DET} + 1.0 V" to "−V_{DET} − 1.0 V".
(5) A time that V_{DOUT} requires to reach 2.5 V when V_{SENSE} changes from "+V_{DET} − 1.0 V" to "+V_{DET} + 1.0 V"

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

R3121NxxxA/E/G Product-specific Electrical Characteristics

Product Name	$-V_{DET}$ [V]				
	Ta = 25°C			−40 °C ≤ Ta ≤ 85°C	
	Min.	Typ.	Max.	Min.	Max.
R3121N030x	2.955	3.000	3.045	2.940	3.060
R3121N031x	3.054	3.100	3.146	3.038	3.162
R3121N032x	3.152	3.200	3.248	3.136	3.264
R3121N033x	3.251	3.300	3.349	3.234	3.366
R3121N034x	3.349	3.400	3.451	3.332	3.468
R3121N035x	3.448	3.500	3.552	3.430	3.570
R3121N036x	3.546	3.600	3.654	3.528	3.672
R3121N037x	3.645	3.700	3.755	3.626	3.774
R3121N038x	3.743	3.800	3.857	3.724	3.876
R3121N039x	3.842	3.900	3.958	3.822	3.978
R3121N040x	3.940	4.000	4.060	3.920	4.080
R3121N041x	4.039	4.100	4.161	4.018	4.182
R3121N042x	4.137	4.200	4.263	4.116	4.284
R3121N043x	4.236	4.300	4.364	4.214	4.386
R3121N044x	4.334	4.400	4.466	4.312	4.488
R3121N045x	4.433	4.500	4.567	4.410	4.590
R3121N046x	4.531	4.600	4.669	4.508	4.692
R3121N047x	4.630	4.700	4.770	4.606	4.794
R3121N048x	4.728	4.800	4.872	4.704	4.896
R3121N049x	4.827	4.900	4.973	4.802	4.998
R3121N050x	4.925	5.000	5.075	4.900	5.100
R3121N051x	5.024	5.100	5.176	4.998	5.202
R3121N052x	5.122	5.200	5.278	5.096	5.304
R3121N053x	5.221	5.300	5.379	5.194	5.406
R3121N054x	5.319	5.400	5.481	5.292	5.508
R3121N055x	5.418	5.500	5.582	5.390	5.610
R3121N056x	5.516	5.600	5.684	5.488	5.712
R3121N057x	5.615	5.700	5.785	5.586	5.814
R3121N058x	5.713	5.800	5.887	5.684	5.916
R3121N059x	5.812	5.900	5.988	5.782	6.018
R3121N060x	5.910	6.000	6.090	5.880	6.120
R3121N061x	6.009	6.100	6.191	5.978	6.222
R3121N062x	6.107	6.200	6.293	6.076	6.324
R3121N063x	6.206	6.300	6.394	6.174	6.426
R3121N064x	6.304	6.400	6.496	6.272	6.528
R3121N065x	6.403	6.500	6.597	6.370	6.630
R3121N066x	6.501	6.600	6.699	6.468	6.732
R3121N067x	6.600	6.700	6.800	6.566	6.834
R3121N068x	6.698	6.800	6.902	6.664	6.936
R3121N069x	6.797	6.900	7.003	6.762	7.038

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

R3121NxxxA/E/G Product-specific Electrical Characteristics

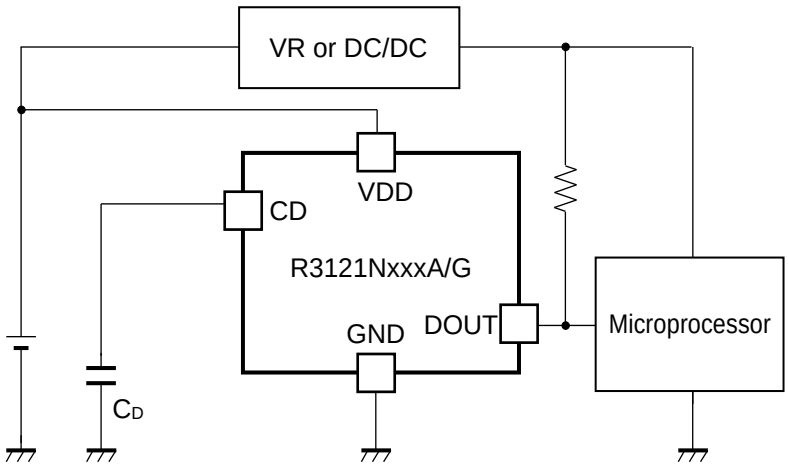
roduct Name	$-V_{DET}$ [V]				
	Ta = 25°C			−40 °C ≤ Ta ≤ 85°C	
	Min.	Typ.	Max.	Min.	Max.
R3121N070x	6.895	7.000	7.105	6.860	7.140
R3121N071x	6.994	7.100	7.206	6.958	7.242
R3121N072x	7.092	7.200	7.308	7.056	7.344
R3121N073x	7.191	7.300	7.409	7.155	7.446
R3121N074x	7.290	7.400	7.511	7.253	7.548
R3121N075x	7.388	7.500	7.612	7.351	7.650
R3121N076x	7.487	7.600	7.714	7.449	7.752
R3121N077x	7.585	7.700	7.815	7.547	7.854
R3121N078x	7.684	7.800	7.917	7.645	7.956
R3121N079x	7.782	7.900	8.018	7.743	8.058
R3121N080x	7.881	8.000	8.120	7.841	8.160
R3121N081x	7.979	8.100	8.221	7.939	8.262
R3121N082x	8.078	8.200	8.323	8.037	8.364
R3121N083x	8.176	3121	8.424	8.135	8.466
R3121N084x	8.275	8.400	8.526	8.233	8.568
R3121N085x	8.373	8.500	8.627	8.331	8.670
R3121N086x	8.472	8.600	8.729	8.429	8.772
R3121N087x	8.570	8.700	8.830	8.527	8.874
R3121N088x	8.669	8.800	8.932	8.625	8.976
R3121N089x	8.767	8.900	9.033	8.723	9.078
R3121N090x	8.866	9.000	9.135	8.821	9.180
R3121N091x	8.964	9.100	9.236	8.919	9.282
R3121N092x	9.063	9.200	9.338	9.017	9.384
R3121N093x	9.161	9.300	9.439	9.115	9.486
R3121N094x	9.260	9.400	9.541	9.213	9.588
R3121N095x	9.358	9.500	9.642	9.311	9.690
R3121N096x	9.457	9.600	9.744	9.409	9.792
R3121N097x	9.555	9.700	9.845	9.507	9.894
R3121N098x	9.654	9.800	9.947	9.605	9.996
R3121N099x	9.752	9.900	10.048	9.703	10.098
R3121N100x	9.850	10.000	10.150	9.800	10.200
R3121N101x	9.949	10.100	10.251	9.898	10.302
R3121N102x	10.047	10.200	10.353	9.996	10.404
R3121N103x	10.146	10.300	10.454	10.094	10.506
R3121N104x	10.244	10.400	10.556	10.192	10.608
R3121N105x	10.343	10.500	10.657	10.290	10.710
R3121N106x	10.441	10.600	10.759	10.388	10.812
R3121N107x	10.540	10.700	10.860	10.486	10.914
R3121N108x	10.638	10.800	10.962	10.584	11.016
R3121N109x	10.737	10.900	11.063	10.682	11.118

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

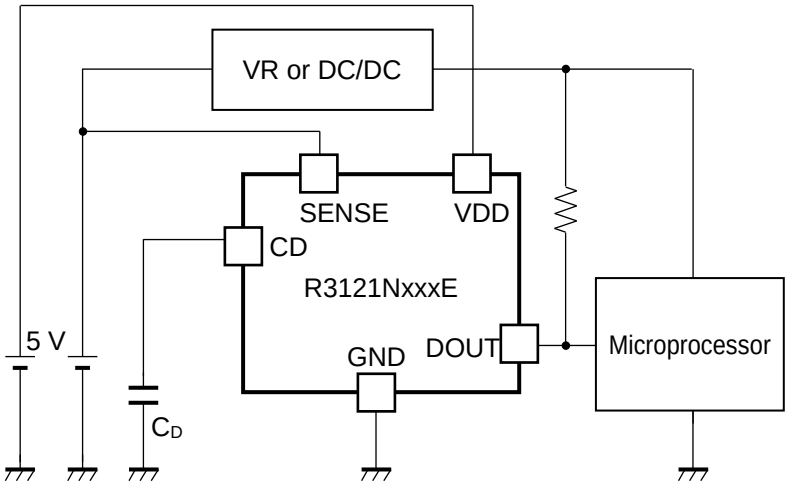
R3121NxxxA/E/G Product-specific Electrical Characteristics

Product Name	$-V_{DET}$ [V]				
	Ta = 25°C			−40 °C ≤ Ta ≤ 85°C	
	Min.	Typ.	Max.	Min.	Max.
R3121N101x	10.835	11.000	11.165	10.780	11.220
R3121N110x	10.934	11.100	11.266	10.878	11.322
R3121N111x	11.032	11.200	11.368	10.976	11.424
R3121N112x	11.131	11.300	11.469	11.074	11.526
R3121N113x	11.229	11.400	11.571	11.172	11.628
R3121N114x	11.328	11.500	11.672	11.270	11.730
R3121N115x	11.426	11.600	11.774	11.368	11.832
R3121N116x	11.525	11.700	11.875	11.466	11.934
R3121N117x	11.623	11.800	11.977	11.564	12.036
R3121N118x	11.722	11.900	12.078	11.662	12.138
R3121N120x	11.820	12.000	12.180	11.760	12.240

TYPICAL APPLICATION CIRCUIT



R3121NxxxA/G Typical Application Circuit



R3121NxxxE Typical Application Circuit

THEORY OF OPERATION

R3121NxxxA (VDD Pin Detection Type)

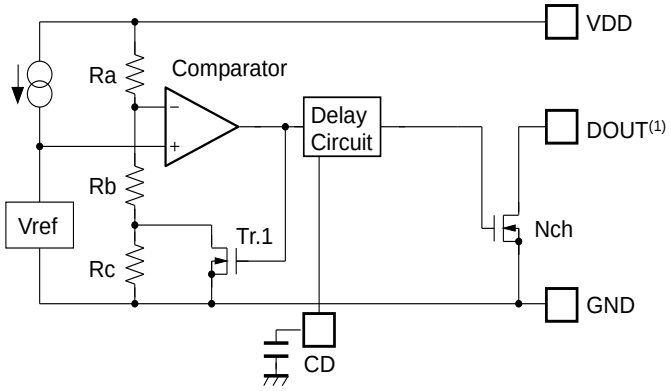
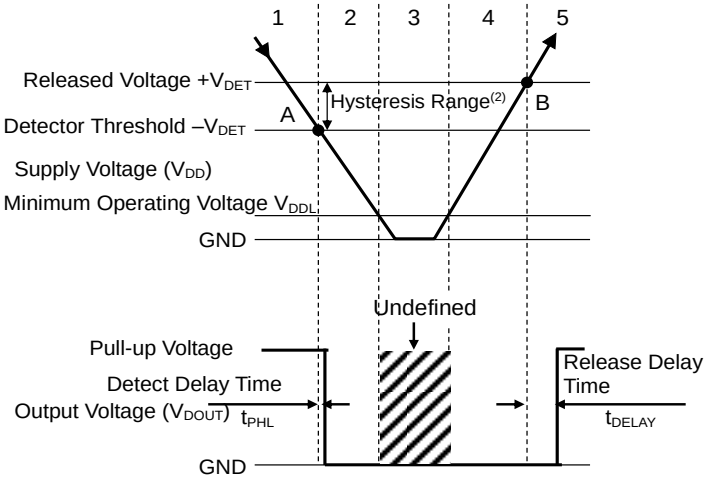


Diagram for R3121NxxxA with External Capacitor



Operating Condition	1	2	3	4	5
Comparator (-) pin Input Voltage	I	II	II	II	I
Comparator Output	L	H	Undefined	H	L
Tr.1	OFF	ON	Undefined	ON	OFF
Output Tr. (Nch)	OFF	ON	Undefined	ON	OFF

$$\text{I} \quad \frac{Rb + Rc}{Ra + Rb + Rc} \times V_{DD}$$

$$\text{II} \quad \frac{Rb}{Ra + Rb} \times V_{DD}$$

R3121NxxxA Operation

OPERATION

1. The output voltage is equal to the pull-up voltage.
2. At A point, Vref ≥ V_{DD} x (Rb+Rc) / (Ra+Rb+Rc) is true. So, the comparator output voltage will be reversed from “L” to “H”. As a result, the output voltage will be “L”.
3. If the supply voltage remains lower than the minimum operating voltage, the output voltage will be undefined.
4. The “L” voltage is output.
5. At B point, Vref ≤ V_{DD} x Rb / (Ra+Rb) is true. So, the comparator output voltage will be reversed from “H” to “L”. As a result, output voltage will be equal to the pull-up voltage.

(1) The DOUT pin should be pulled-up to VDD pin or an external voltage level.
(2) Hysteresis is a voltage difference between the released voltage and the detector threshold.

● **R3121NxxxG (VDD Pin Detection Type)**

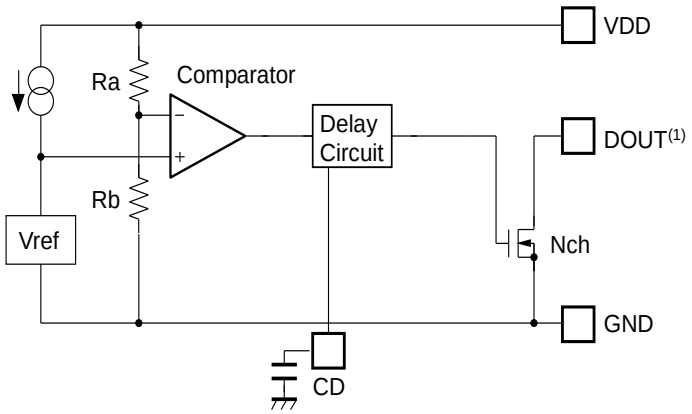
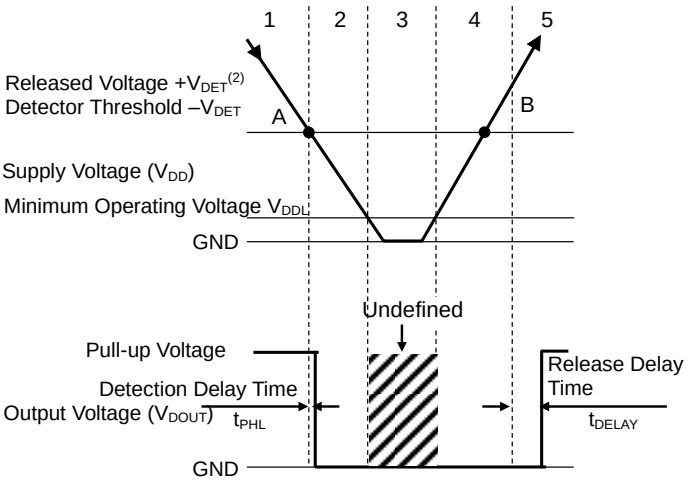


Diagram for R3121NxxxG with External Capacitor



Operating Condition	1	2	3	4	5
Comparator (-) pin Input Voltage	I	I	I	I	I
Comparator Output	L	H	Undefined	H	L
Tr.1	OFF	ON	Undefined	ON	OFF
Output Tr. (Nch)	OFF	ON	Undefined	ON	OFF

$$I \quad \frac{Rb}{Ra + Rb} \quad x\ V_{DD}$$

R3121NxxxG Operation

OPERATION

1. The output voltage is equal to the pull-up voltage.
2. At A point, Vref ≥ V_{DD} x Rb / (Ra+Rb) is true. So, the comparator output voltage will be reversed from “L” to “H”. As a result, the output voltage will be “L”.
3. If the supply voltage remains lower than the minimum operating voltage, the output voltage will be undefined.
4. The “L” voltage is output.
5. At B point, Vref ≤ V_{DD} x Rb / (Ra+Rb) is true. So, the comparator output voltage will be reversed from “H” to “L”. As a result, output voltage will be equal to the pull-up voltage.

(1) The DOUT pin should be pulled-up to VDD pin or an external voltage level.
(2) As for R3121NxxxG, whether or not Chattering may occur at detecting / Release depends on the tilt of supply voltage fluctuations. If the chattering becomes a problem, connect a capacitor of 10nF or more with the CD pin.

R3121xxxE (SENSE Pin Detection Type)

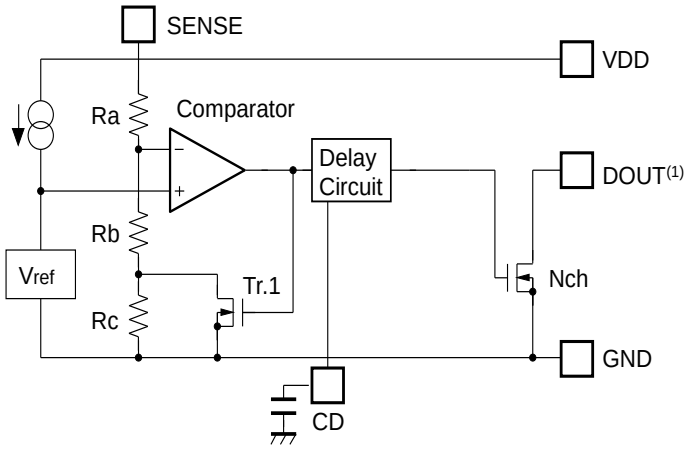
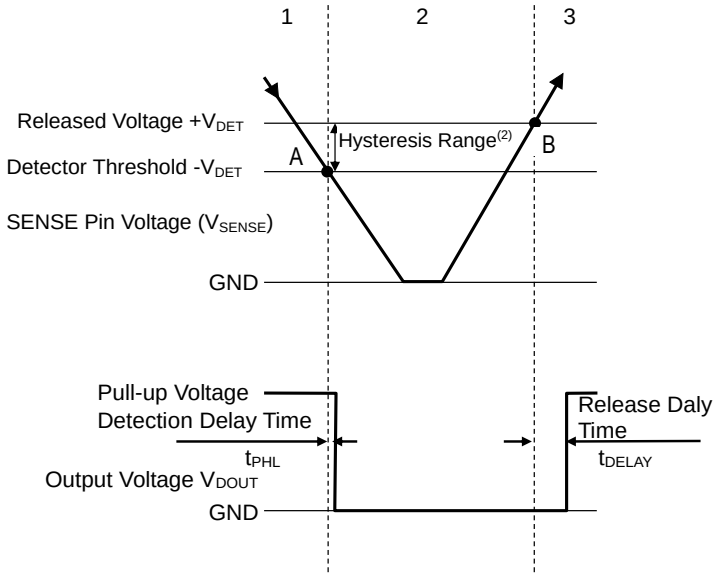


Diagram for R3121xxxE with External Capacitor



Operating Condition	1	2	3
Comparator (-) pin Input voltage	I	II	I
Comparator Output	L	H	L
Tr.1	OFF	ON	OFF
Output Tr. (Nch)	OFF	ON	OFF

$$\text{I} \quad \frac{Rb + Rc}{Ra + Rb + Rc} \times V_{SENSE}$$

$$\text{II} \quad \frac{Rb}{Ra + Rb} \times V_{SENSE}$$

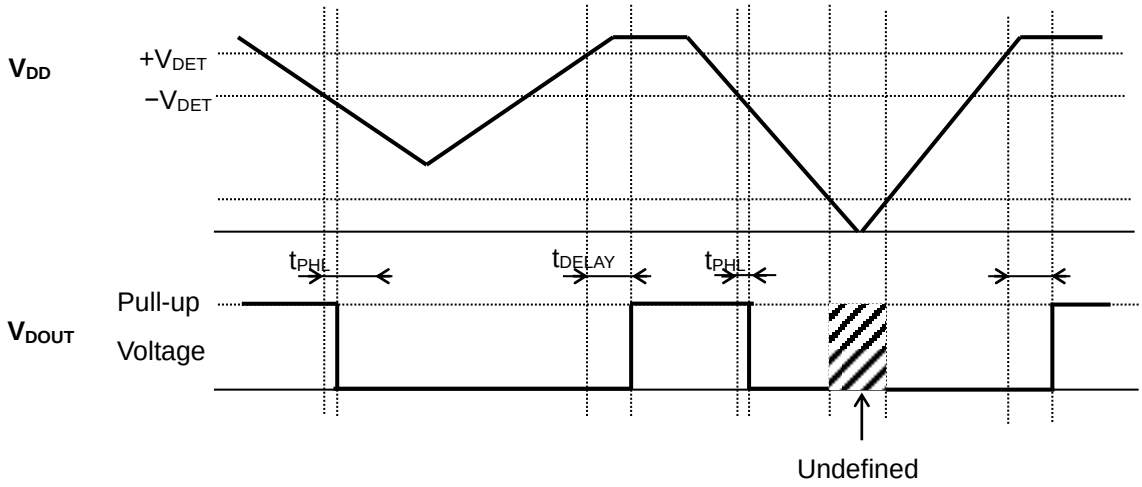
R3121NxxxE Operation

OPERATION

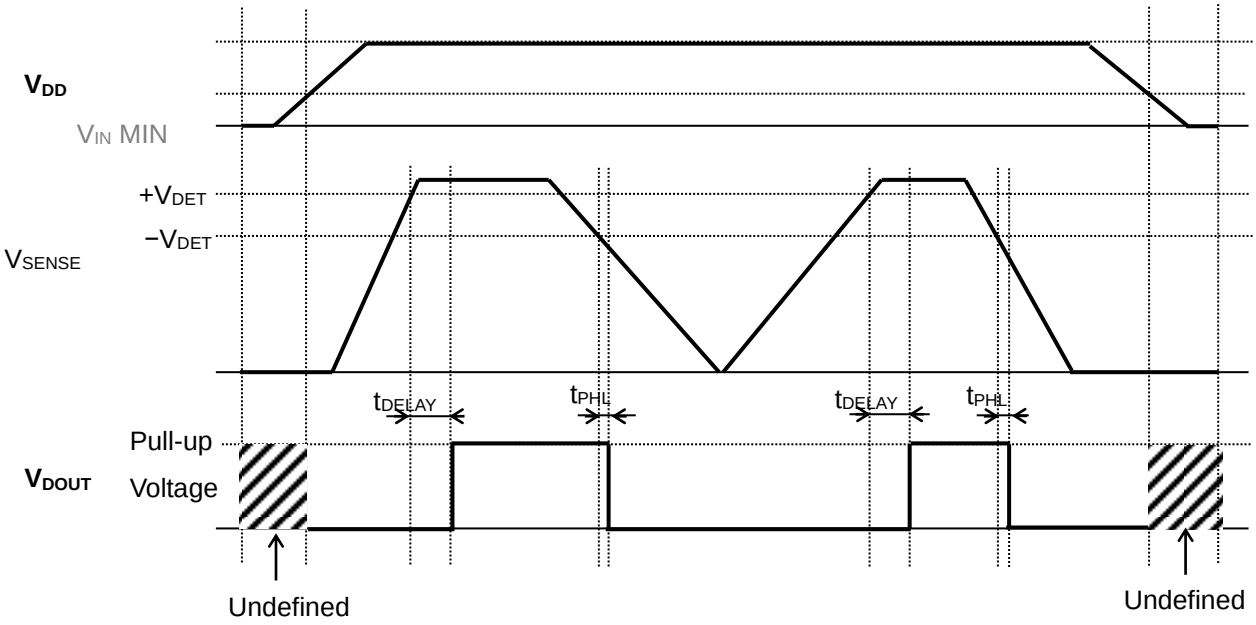
1. The SENSE pin voltage is higher than the detector threshold; the output voltage is equal to the pull-up voltage.
2. At A point, Vref ≥ V_{SENSE} x (Rb+Rc) / (Ra+Rb+Rc) is true. So, the comparator output voltage will be reversed from “L” to “H”. As a result, the output voltage will be “L”. If the supply voltage remains higher than the minimum operating voltage, the output voltage will stay in “L”.
3. At B point, Vref ≤ V_{SENSE} x Rb / (Ra+Rb) is true. So, the comparator output voltage will be reversed from “H” to “L”. As a result, output voltage will be equal to the pull-up voltage.

(1) The DOUT pin should be pulled-up to an external voltage level.
(2) Hysteresis is a voltage difference between the released voltage and the detector threshold.

TIMING CHARTS



R3121NxxxA/R3121NxxxG (VDD Pin Detection Type)



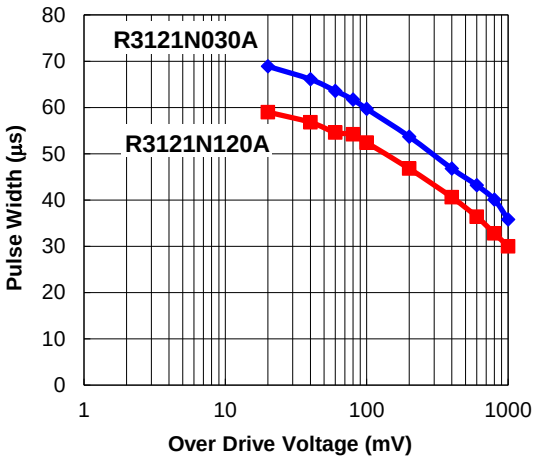
R3121NxxxE (SENSE Pin Detection Type)

POWER SEQUENCE

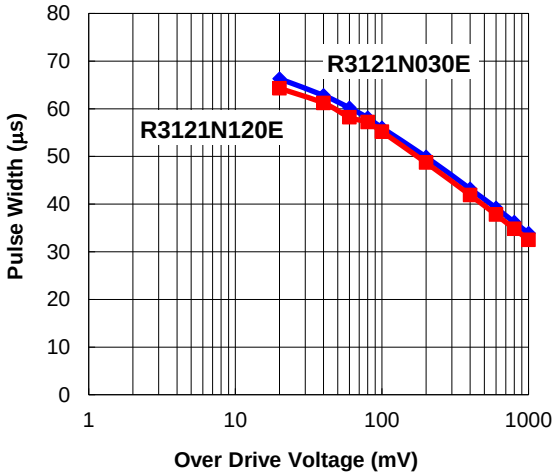
The R3121NxxxE is a SENSE pin voltage detection type which supervises the SENSE pin voltage. When powering up, either the VDD pin or the SENSE pin can power up first. In the case of powering up the VDD pin from the minimum voltage or lower, after the powering up of the SENSE pin, the VDD pin have to be powered up 10 V/ms or less. In the case of powering down the VDD pin, the SENSE pin has to be powered down first. After the detection delay time (t_{RESET}), the VDD pin has to be powered down.

GLITCH DETECTION by VDD and SENSE PINS

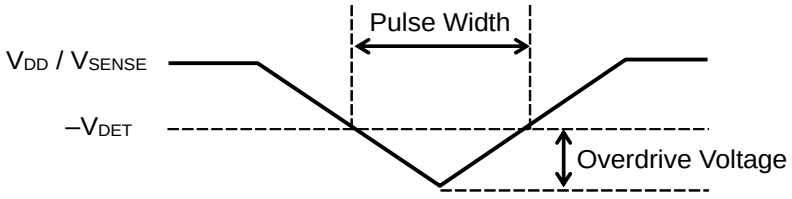
The following graphs are the released conditions when a pulse voltage less than or equal to the detector threshold ($-V_{DET}$) is applied to VDD (R3121NxxxA/G) / VSENSE (R3121NxxxE) pin during the release operation. The graphs indicate the maximum pulse condition. If a pulse increased in width and voltage is applied to V_{DD} (R3121NxxxA/G) / V_{SENSE} (R3121NxxxE), the reset signal may occur.



R3121NxxxA/G Pulse Width vs. Over Drive Voltage



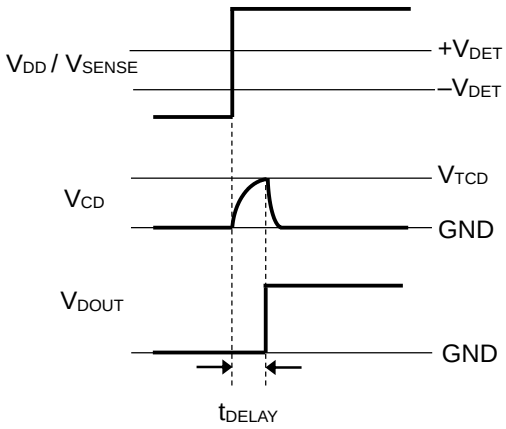
R3121NxxxE Pulse Width vs. Over Drive Voltage



V_{DD}/V_{SENSE} Input Waveform

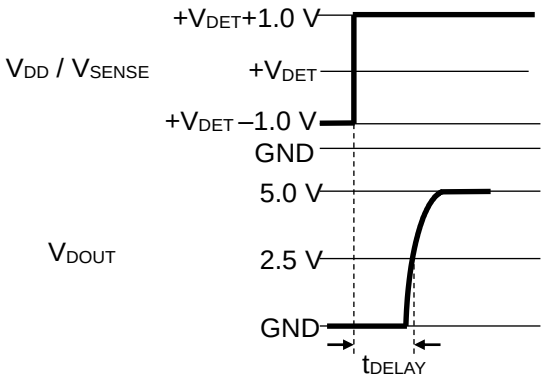
RELEASE DELAY TIME (t_{DELAY})

When the voltage higher than the released voltage is applied to the VDD / SENSE pin while the voltage lower than the detector threshold ($-V_{DET}$) is applied to VDD/ SENSE pin, charging the external capacitor starts and the CD pin voltage (V_{CD}) is increased. The output voltage maintains the released output until V_{CD} reaches the threshold voltage of the release output delay pin (V_{TCD}). And when V_{CD} exceeds V_{TCD}, the output voltage is inverted from the detected output to the released output. That is, the charged external capacitor starts discharging.



R3121NxxxA/E/G Released Delay Time

Release Delay Time (t_{DELAY}) indicates the time between the instance when V_{DD} / V_{SENSE} shift from "$+V_{DET}$ -1.0 V" to "$+V_{DET}$+1.0 V" by the application of a pulse voltage and the instance when the output voltage reaches 2.5 V after pulled up the output pin (D_{OUT}) to 5.0 V with a resistor of 100 kΩ.
This is given by the expression t_{DELAY} (s) = C_D x 10^7, where C_D (F) represents capacitance of the external capacitor.



R3121NxxxA/E/G Released Delay Time

TECHNICAL NOTES

When connecting resistors to VDD pin

When connecting a resistor (R1) to VDD pin, the input voltage decreases by [Device's Consumption Current] x [Resistance Value] only. And, the cross conduction current (1), which occurs when changing from the detecting state to the release state, is decreased the input voltage by [Cross Conduction Current] x [Resistance Value] only. And then, this device will enter the re-detecting state if the input voltage reduction is larger than the difference between the detector voltage and the released voltage.
When the input resistance value is large and the V_{DD} is gone up at mildly in the vicinity of the released voltage, repeating the above operation may result in the occurrence of output.

As shown in Figure A/B, set R1 to become 100 kΩ or less as a guide, and connect C_{IN} of 0.1 μF and more to between the input pin and GND. Besides, make evaluations including temperature properties under the actual usage condition, with using the evaluation board like this way. As result, make sure that the cross conduction current has no problem.

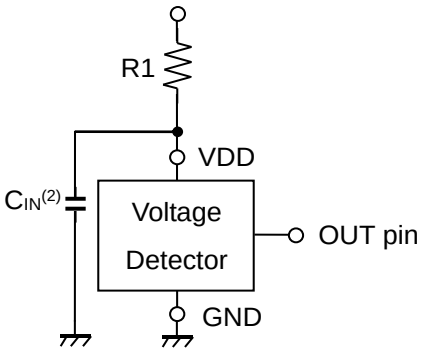


図 A

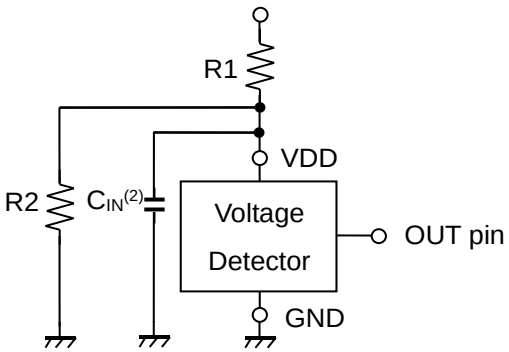


図 B

(1) In the CMOS output type, a charging current for OUT pin is included.
(2) Note the bias dependence of capacitors.

Prohibited Area of Supply Voltage Fluctuations (VDD Pin Detection Type)

As for the steep change of the supply voltages in the prohibited area as shown in Figure C, the detector may cause a false detection if the supply voltage is over the detector threshold, as shown in Figure D.

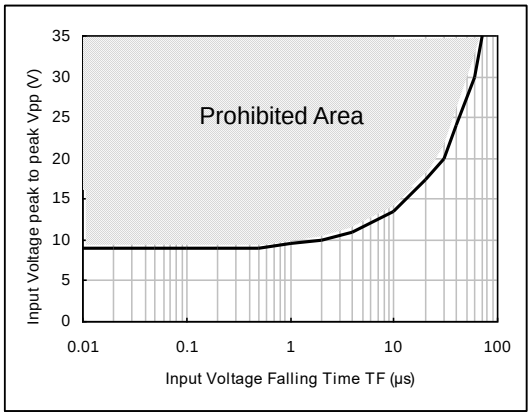


Figure C: Prohibited Area

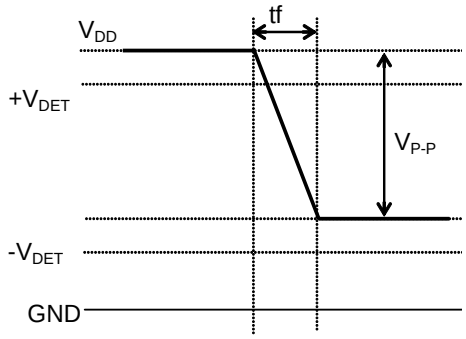


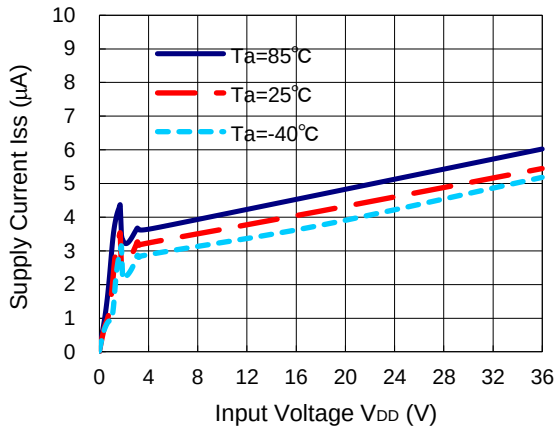
Figure D

TYPICAL CHARACTERISTICS

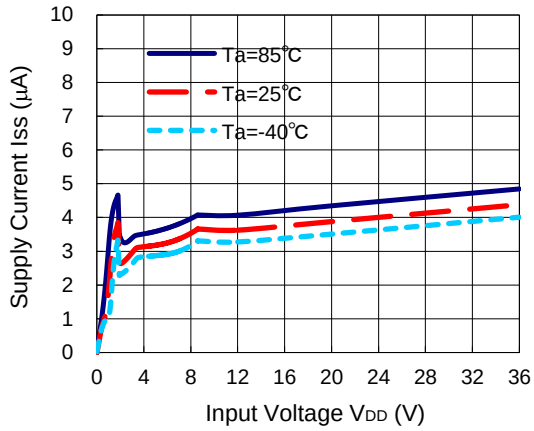
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Supply Current vs. Input Voltage

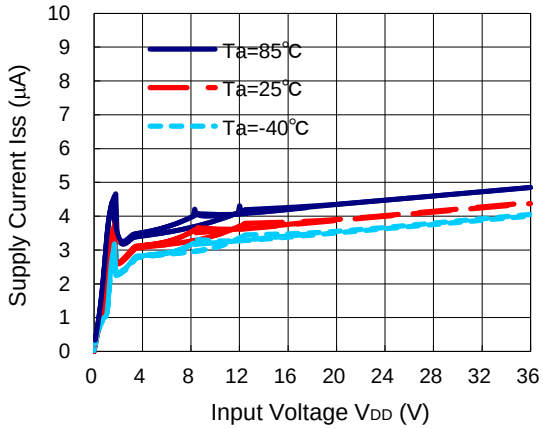
R3121N030A/G



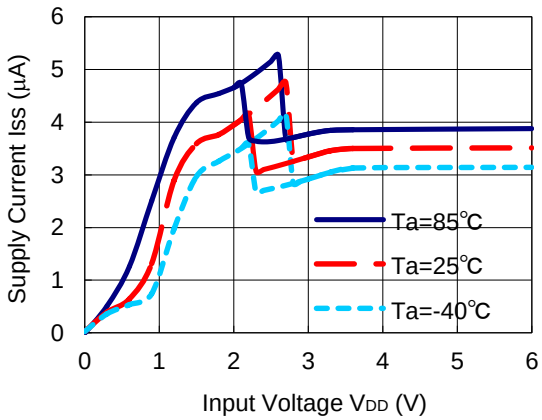
R3121N083A/G



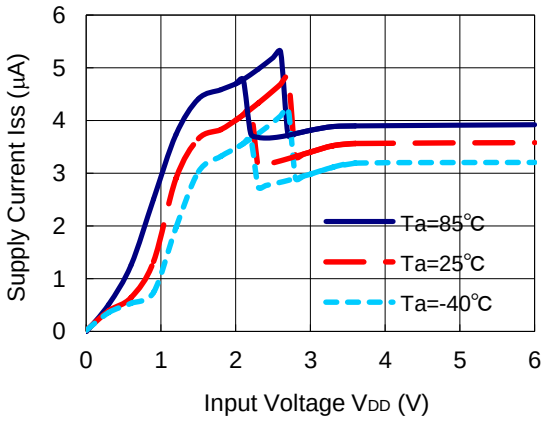
R3121N120A/G



R3121NxxxE (V_{SENSE} = -V_{DET} -0.1V)

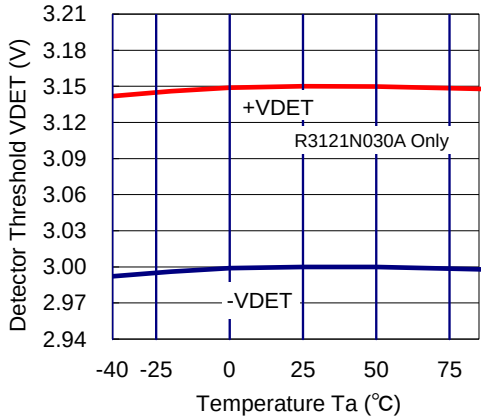


R3121NxxxE(V_{SENSE} = +V_{DET}-+0.1V)

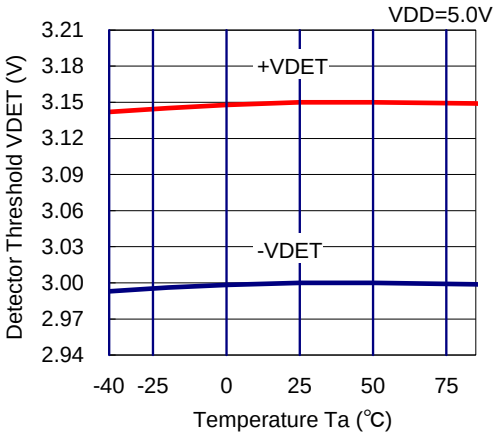


2) Detector Threshold vs. Temperature

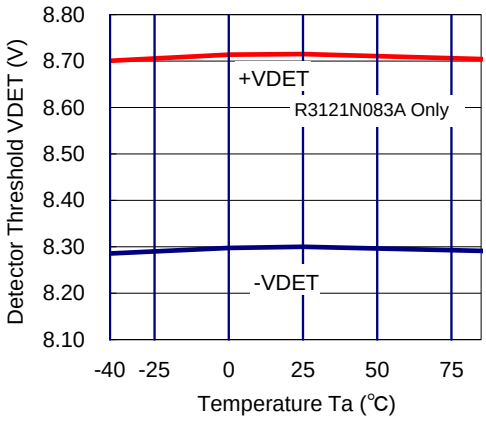
R3121N030A/G



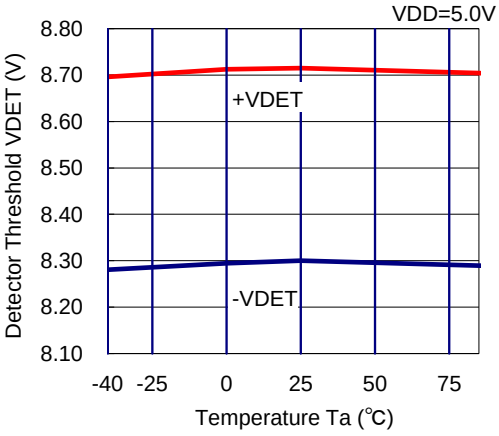
R3121N030E



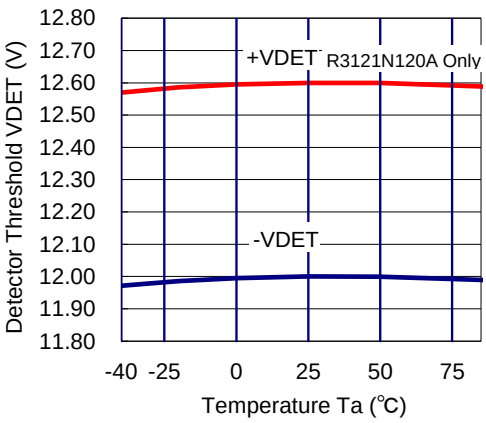
R3121N083A/G



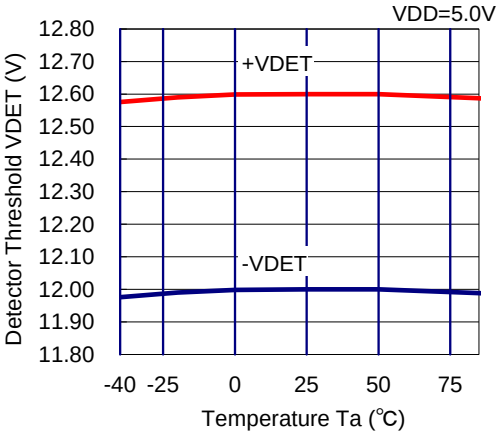
R3121N083E



R3121N120A/G

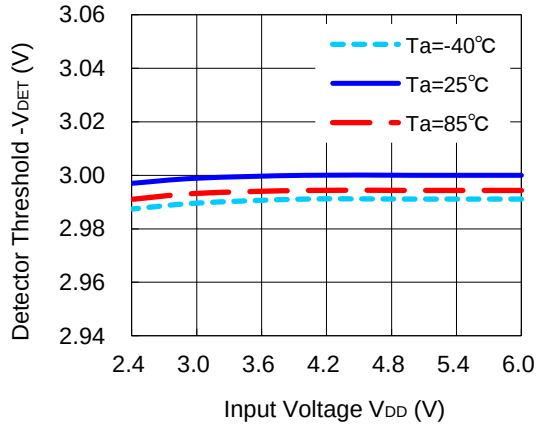


R3121N120E

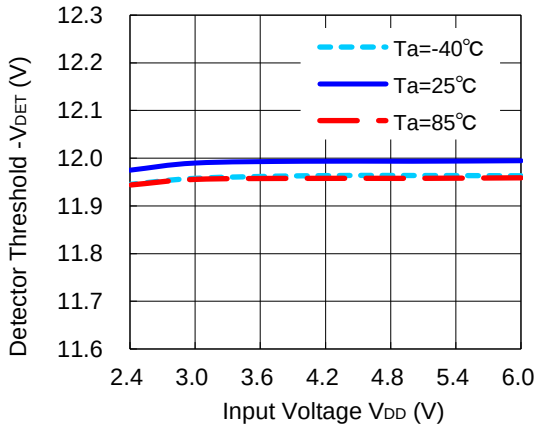


3) Detector Threshold vs. Input Voltage

R3121N030E

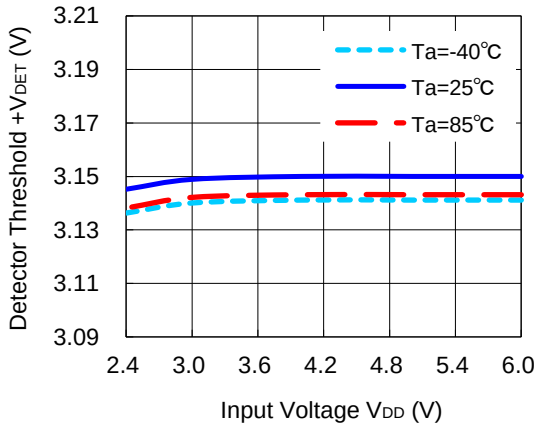


R3121N120E

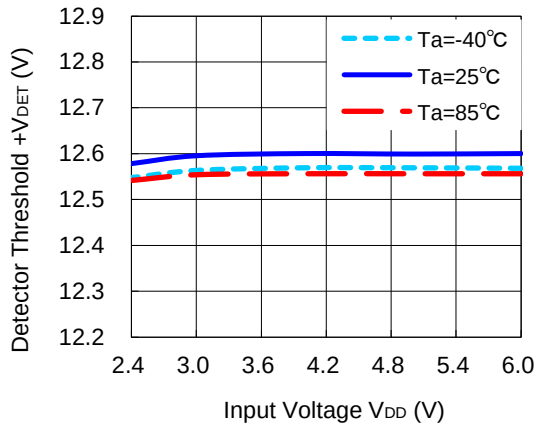


4) Release Voltage vs. Input Voltage

R3121N030E

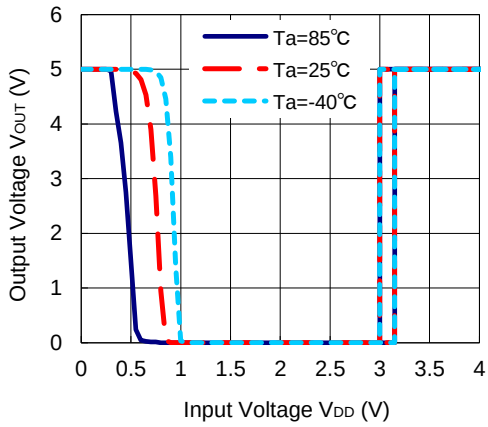


R3121N120E

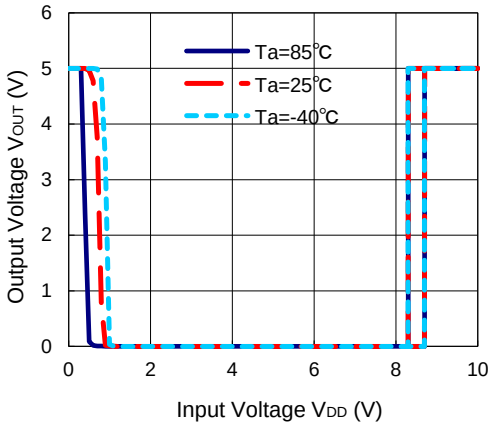


5) Output Voltage vs. Input Voltage (Ta = 25°C, D_{OUT}: pulled-up to 5.0 V with 100 kΩ)

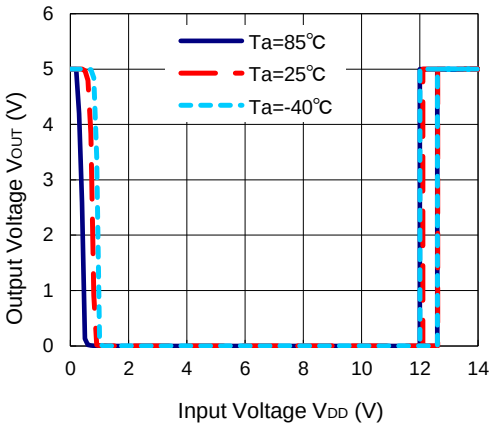
R3121N030A



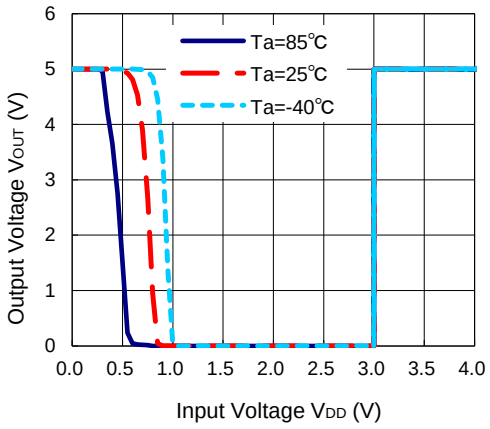
R3121N083A



R3121N120A

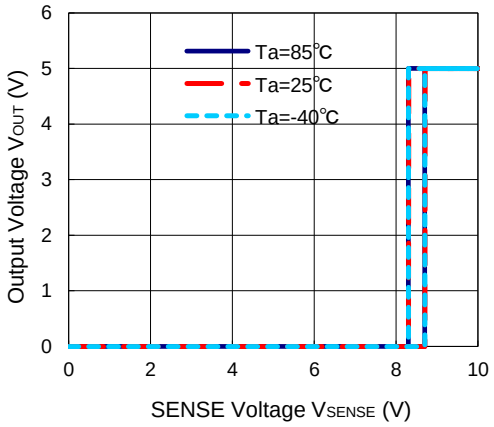


R3121N030G

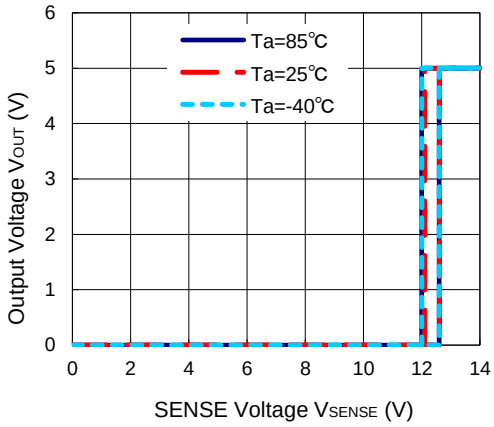


6) Output Voltage vs. SENSE Pin Voltage (V_{DD} = 5.0 V, D_{OUT}: pulled-up to 5.0 V with 100 kΩ)

R3121N083E

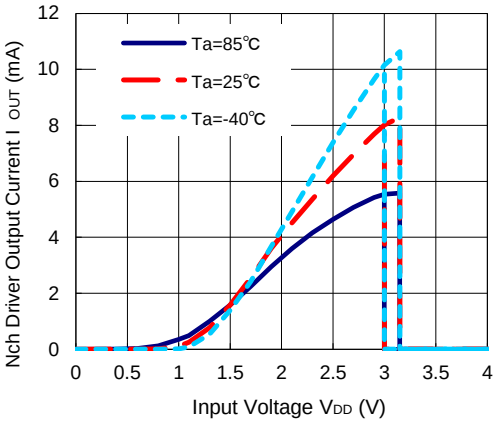


R3121N120E

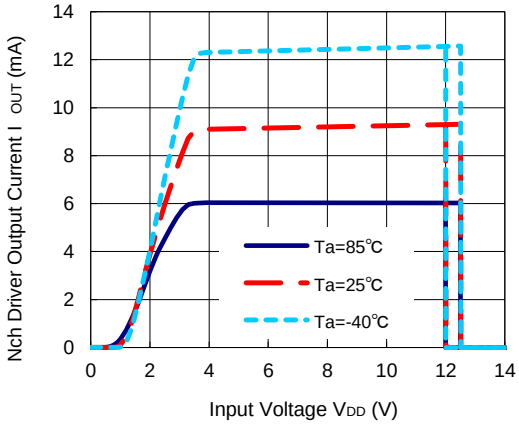


7) Nch. Driver Output Current vs. Input Voltage

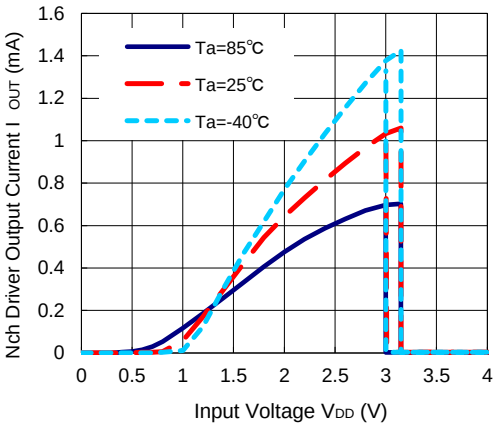
R3121N030A
(V_{DOUT}=0.5V)



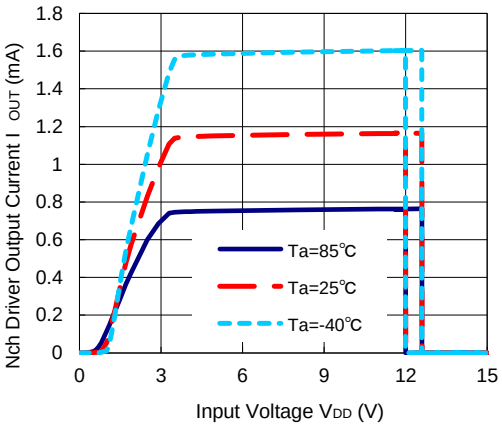
R3121N120A
(V_{DOUT}=0.5V)



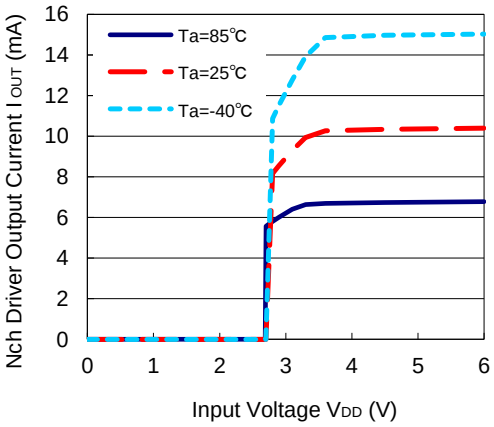
R3121N030A
(V_{DOUT}=0.05V)



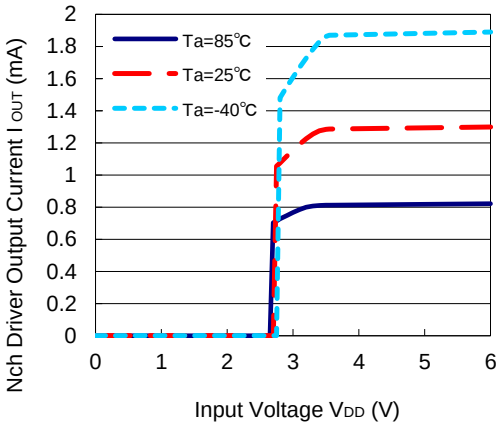
R3121N120A
(V_{DOUT}=0.05V)



R3121NxxxE
(V_{SENSE} = -V_{DET} - 1.0V,V_{DOUT}=0.5V)

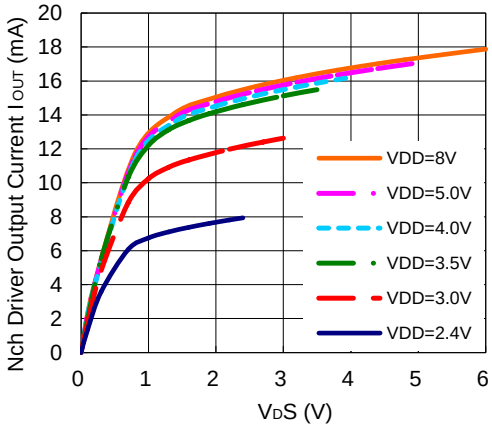


R3121NxxxE
(V_{SENSE} = -V_{DET} -1.0V,V_{DOUT}=0.05V)

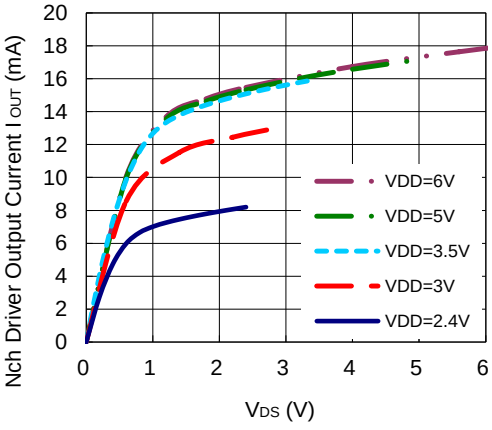


8) Nch. Driver Output Current vs. V_{DS} (Ta = 25°C)

R3121NxxxA/G

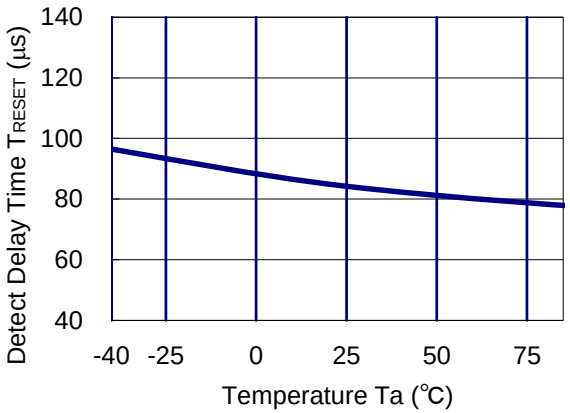


R3121NxxxE

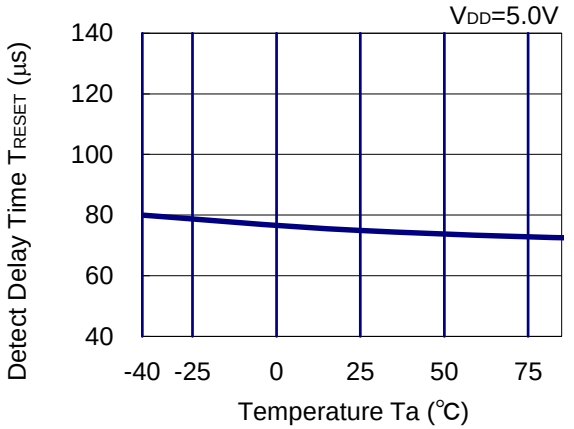


9) Detection Delay Time vs. Temperature

R3121NxxxA/G

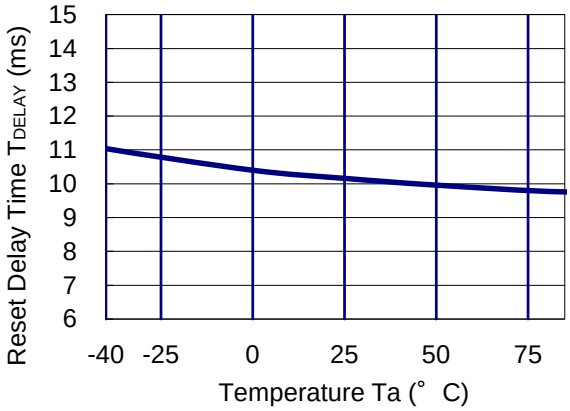


R3121NxxxE

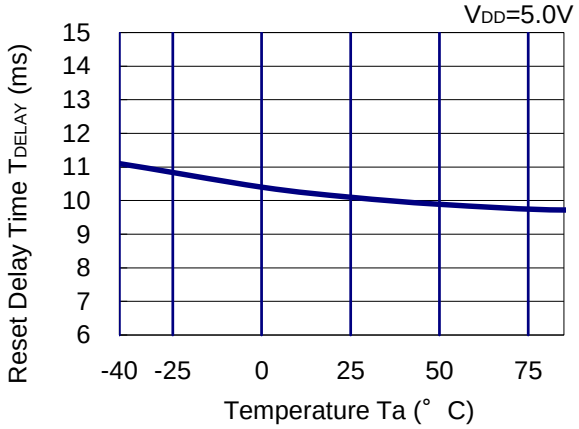


10) Release Delay Time vs. Temperature (C_D = 1.0 µF)

R3121NxxxA/G

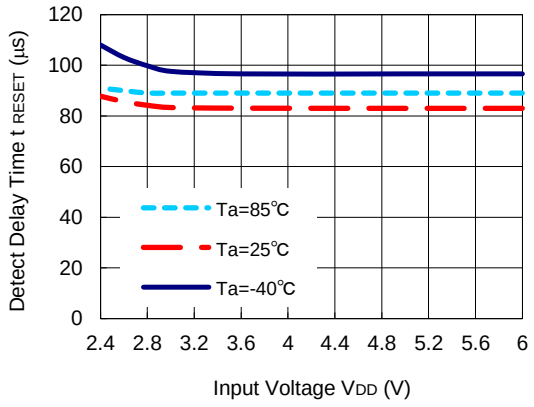


R3121NxxxE



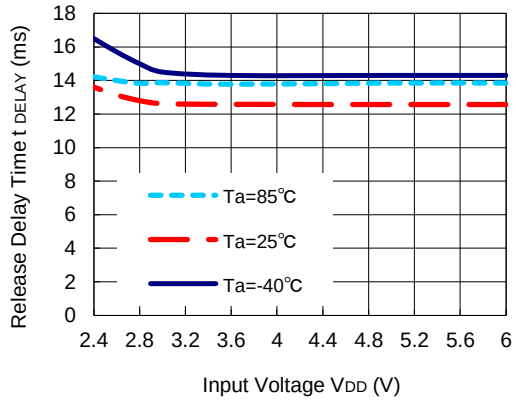
11) Detection Delay Time vs. Input Voltage

R3121NxxxE



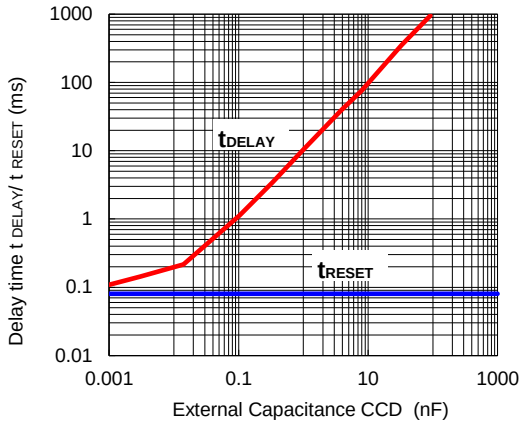
12) Release Delay Time vs. Input Voltage

R3121NxxxE

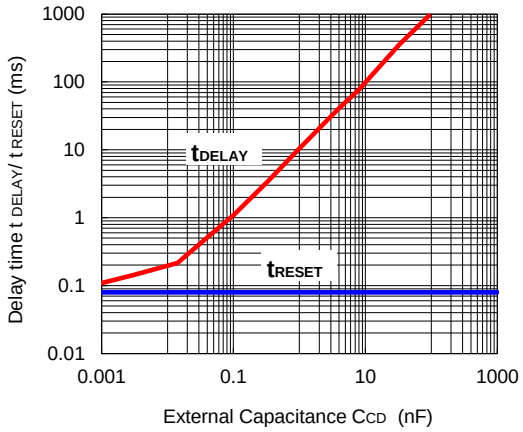


13) Release Delay Time vs. External Capacitor for CD Pin (Ta = 25°C)

R3121NxxxA/G



R3121NxxxE



Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

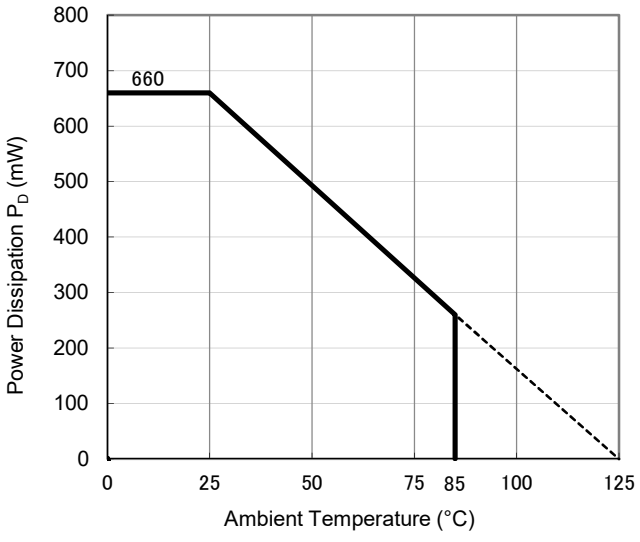
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 7 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

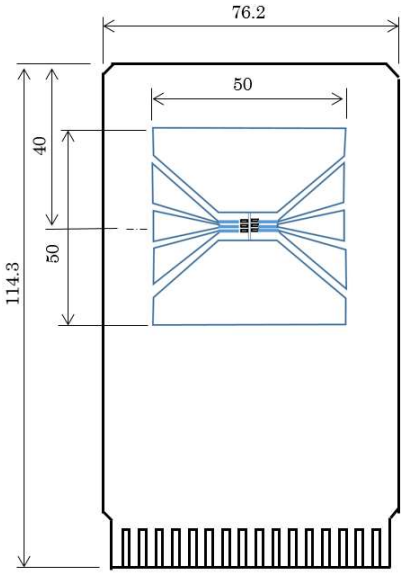
Item	Measurement Result
Power Dissipation	660 mW
Thermal Resistance (θja)	θja = 150°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 51°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

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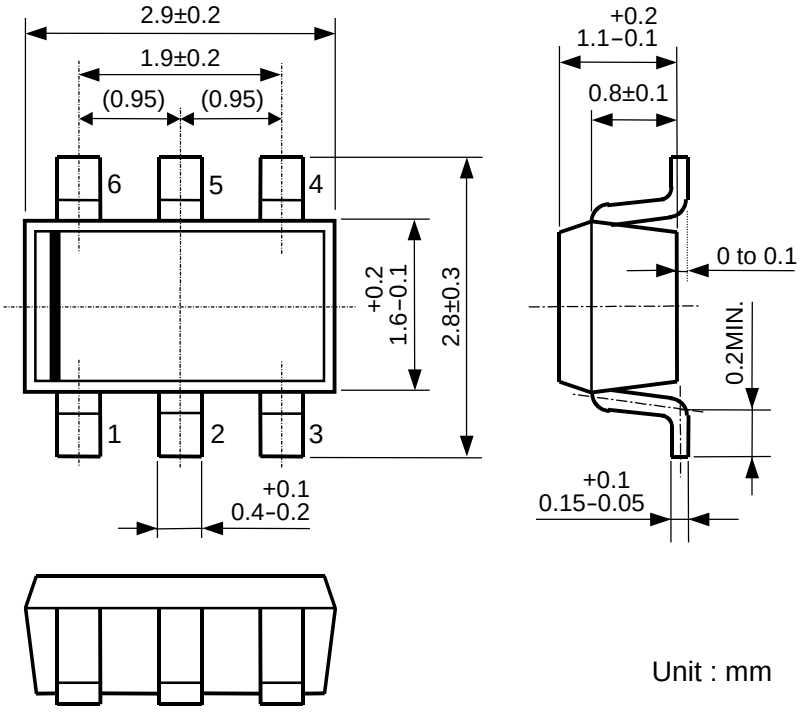
Ver. A



Unit : mm

SOT-23-6 Package Dimensions

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Sales & Support Offices

Ricoh Electronic Devices Co., Ltd.
Shin-Yokohama Office (International Sales)
2-3, Shin-Yokohama 3-chome, Kohoku-ku, Yokohama-shi, Kanagawa, 222-8530, Japan
Phone: +81-50-3814-7687 Fax: +81-45-474-0074

Ricoh Americas Holdings, Inc.
675 Campbell Technology Parkway, Suite 200 Campbell, CA 95008, U.S.A.
Phone: +1-408-610-3105

Ricoh Europe (Netherlands) B.V.
Semiconductor Support Centre
Prof. W.H. Keesomlaan 1, 1183 DJ Amstelveen, The Netherlands
Phone: +31-20-5474-309

Ricoh International B.V. - German Branch
Semiconductor Sales and Support Centre
Oberrather Strasse 6, 40472 Düsseldorf, Germany
Phone: +49-211-6546-0

Ricoh Electronic Devices Korea Co., Ltd.
3F, Haesung Bldg, 504, Teheran-ro, Gangnam-gu, Seoul, 135-725, Korea
Phone: +82-2-2135-5700 Fax: +82-2-2051-5713

Ricoh Electronic Devices Shanghai Co., Ltd.
Room 403, No.2 Building, No.690 Bibo Road, Pu Dong New District, Shanghai 201203, People's Republic of China
Phone: +86-21-5027-3200 Fax: +86-21-5027-3299

Ricoh Electronic Devices Shanghai Co., Ltd.
Shenzhen Branch
1205, Block D(Jinlong Building), Kingkey 100, Hongbao Road, Luohu District, Shenzhen, China
Phone: +86-755-8348-7600 Ext 225

Ricoh Electronic Devices Co., Ltd.
Taipei office
Room 109, 10F-1, No.51, Hengyang Rd., Taipei City, Taiwan
Phone: +886-2-2313-1621/1622 Fax: +886-2-2313-1623