ME2328/ME2328-G

N - Channel 105-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2328 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

- $R_{DS(ON)} \leqq 270m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 340m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

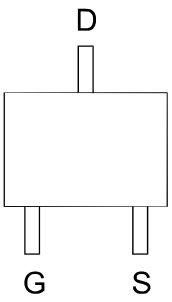
APPLICATIONS

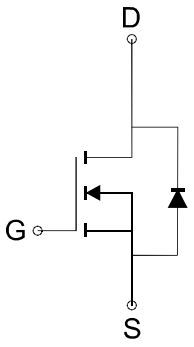
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOT-23)

Top View





N-Channel MOSFET

Ordering Information: ME2328(Pb-free)

ME2328-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	105	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_j=150℃)	T_A=25℃	I_D	1.5	A
	T_A=70℃		1.2	
Pulsed Drain Current		I_{DM}	6	A
Maximum Power Dissipation	T_A=25℃	P_D	1.3	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

N - Channel 105-V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	105	110		V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1	2	3	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=105V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=1.5A		230	270	mΩ
		V_{GS}=4.5V, I_D=1.0A		275	340	
V_{SD}	Diode Forward Voltage *	I_{SD}=1.0A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=50V, V_{GS}=10V, I_D=1.5A		12		nC
Qg	Total Gate Charge	V_{DS}=50V, V_{GS}=4.5V, I_D=1.5A		6.6		
Qgs	Gate-Source Charge			2.6		
Qgd	Gate-Drain Charge			3.3		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		0.8		Ω
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		326		pF
Coss	Output Capacitance			38		
Crss	Reverse Transfer Capacitance			11		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=50V, R_L=33Ω, I_D=0.2A, V_{GEN}=10V, R_G=6Ω		10		ns
t_r	Turn-On Rise Time			6		
$t_{d(off)}$	Turn-Off Delay Time			30		
t_f	Turn-Off Fall Time			4		

Notes: a, pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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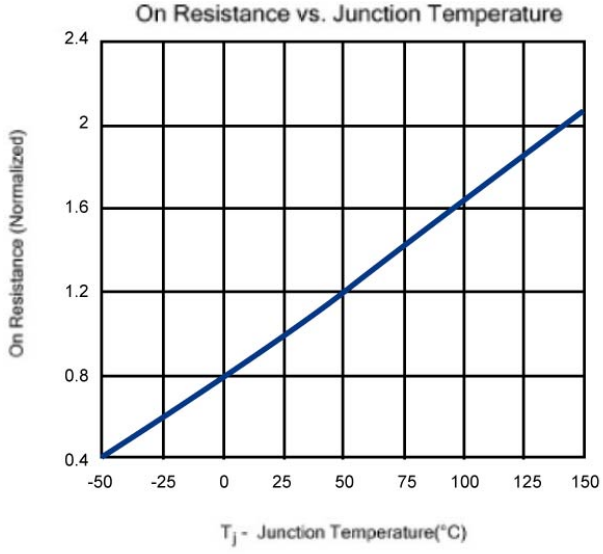
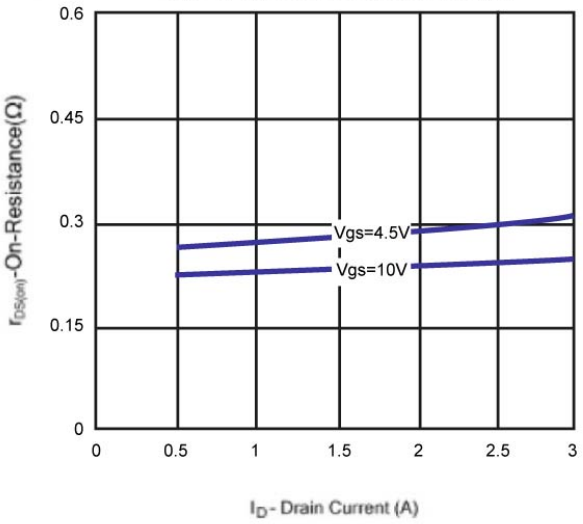
Typical Characteristics (T_J =25℃ Noted)

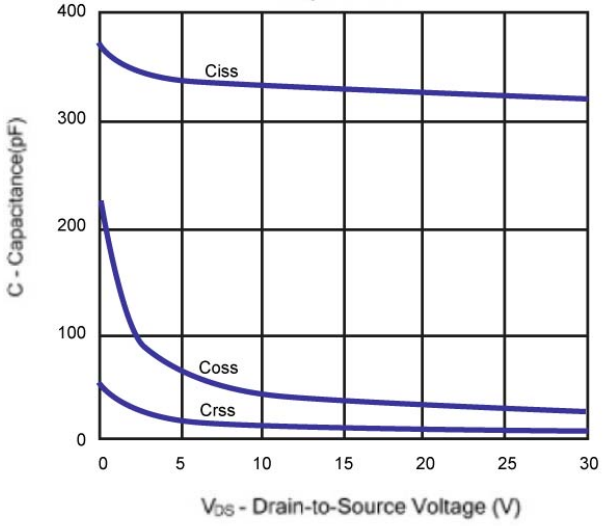
On Resistance vs. Junction Temperature



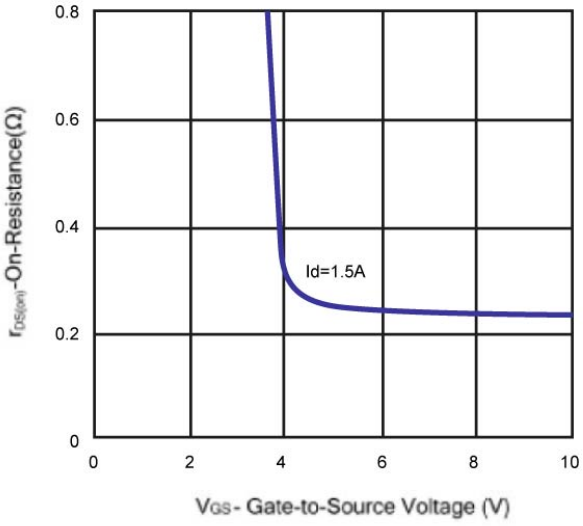
On-Resistance vs. Drain Current



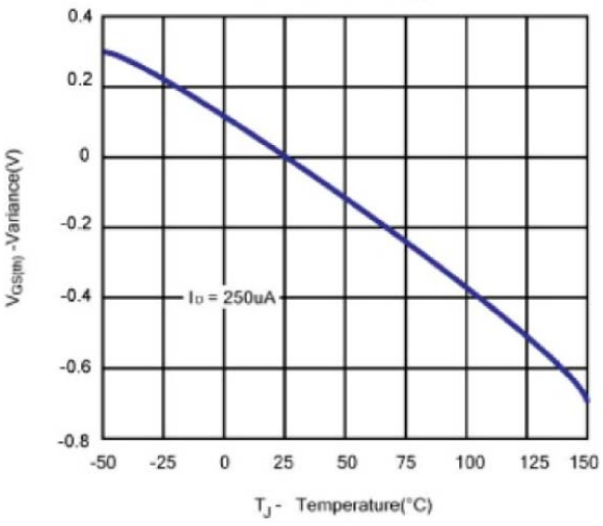
Capacitance



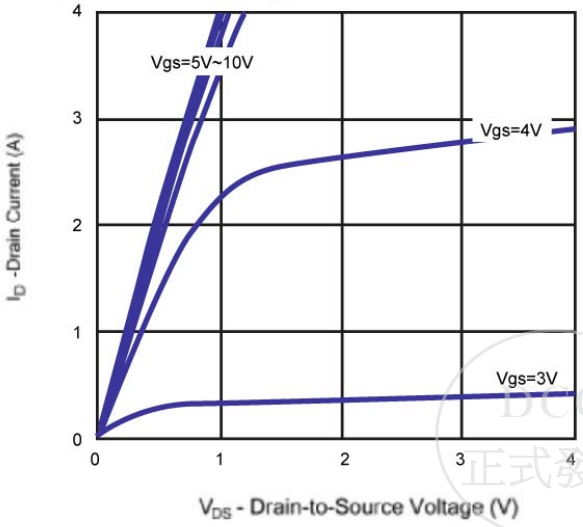
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



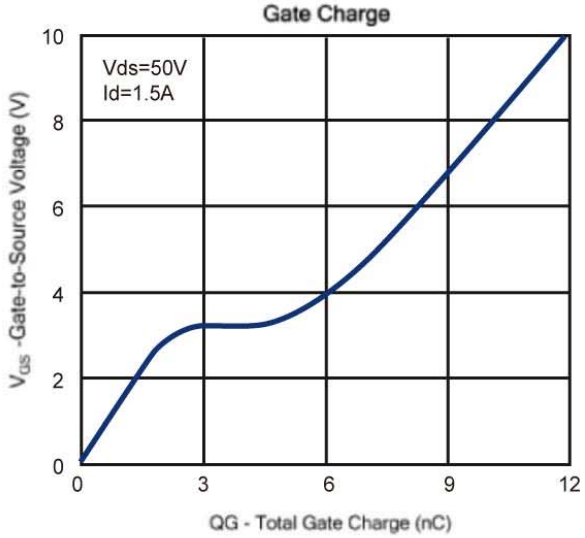
On-Region Characteristics



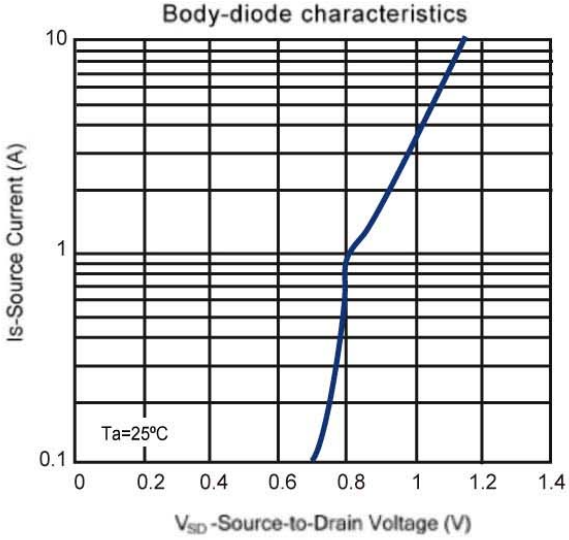
N - Channel 105-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

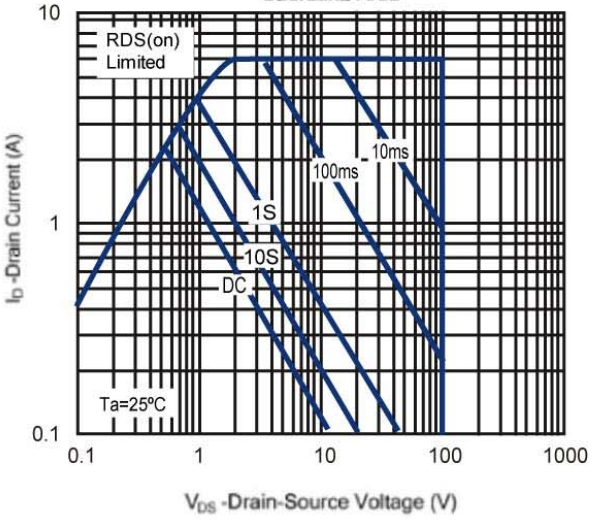
Gate Charge



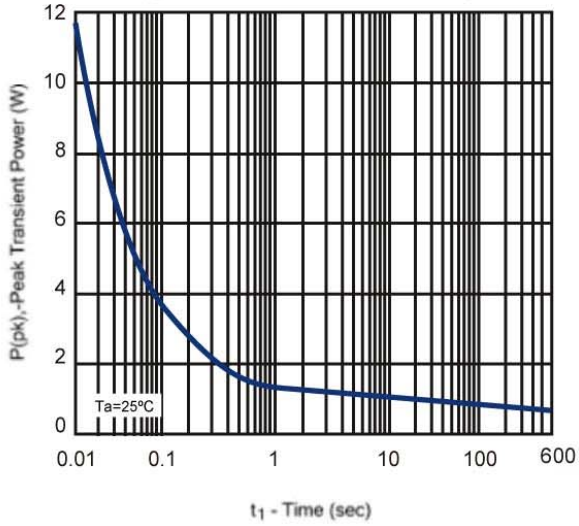
Body-diode characteristics



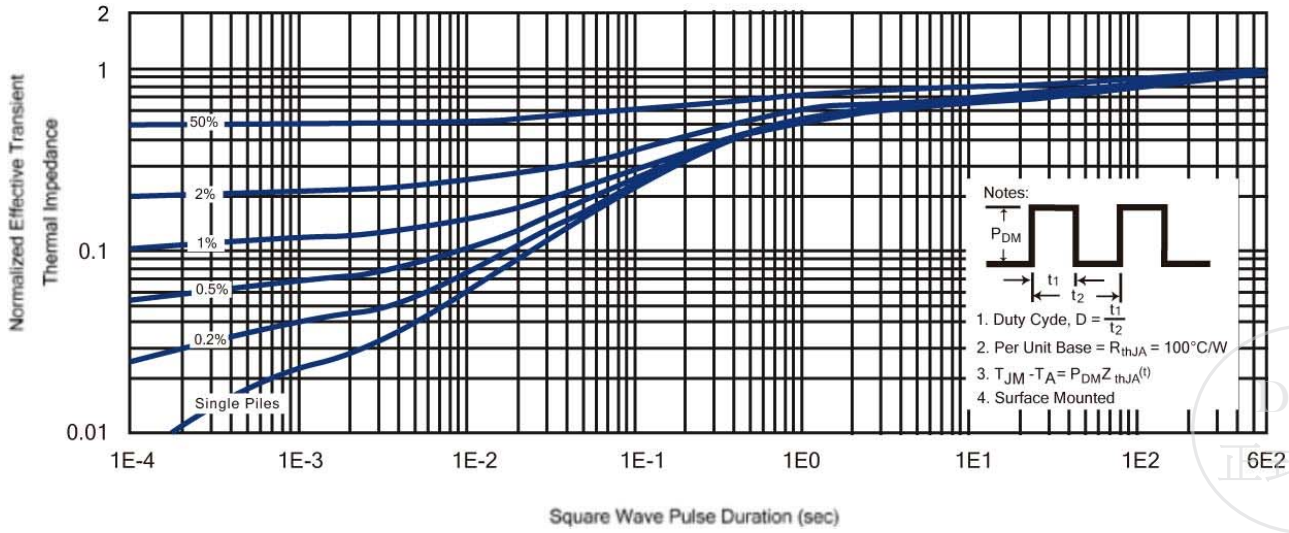
Maximum Forward Biased Safe Operating Area



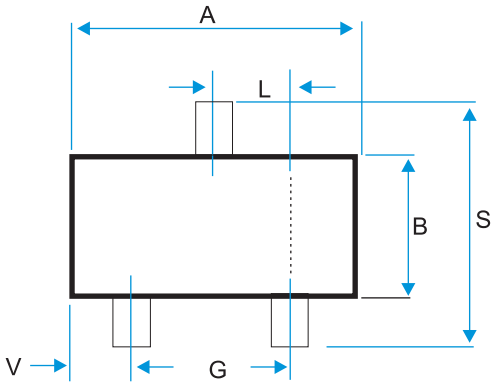
Single Pulse Maximum Power Dissipation

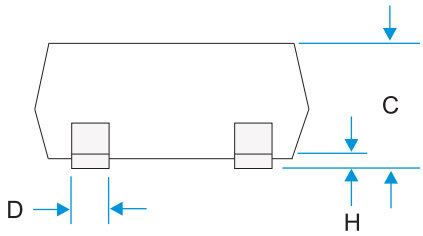


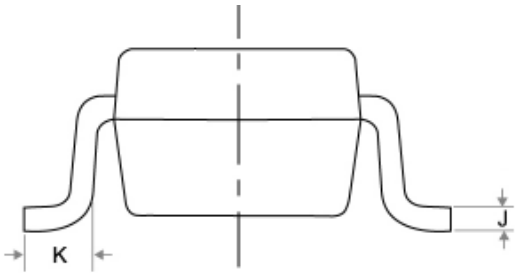
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60